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Specification

Title of the Invention: SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE

What is claimed is:

1. A semiconductor integrated circuit device, in which an MOS field effect transistor is formed taking a polycrystalline silicone formed on an insulating film as a substrate, characterized in that an insulating film of a gate part has a two-layer structure of a silicon oxide film and a silicon nitride film.

2. The semiconductor integrated circuit device according to claim 1, wherein the film thickness of said silicon oxide film ranges from 30Å to 1000Å.

3. The semiconductor integrated circuit device according to claims 1 and 2, wherein the film thickness of said silicon nitride film ranges from 30Å to 1000Å.

Detailed Description of the Invention:

This invention relates to an MOS field effect transistor using a polycrystalline silicon formed on an insulating film as a substrate and particularly to the gate insulating film thereof.

The semiconductor integrated circuit device has been developed into micro-structure with the years, and especially the development of the semiconductor integrated circuit device taking an MOS field effect transistor as a constituent is remarkable.

Aligner technique, etching technique and device technique are further being advanced, and the development of micro-structure reaches below 2 μ rule to get nearer to its limit at the mass production level. A three-dimensional semiconductor integrated circuit device in which elements are stacked up has been conceived far in advance, and various studies have been made in the respective fields. Under these circumstances, suddenly the study is becoming active.

Devices which adopt an MOS field effect transistor as a constituent are now developed. At present, there are many problems in practical applications, and among them, especially the major problem is that the withstanding pressure of a gate part on polycrystalline silicon is low. This results from that when the surface of the polycrystalline silicon is oxidized, the polycrystalline silicon is further crystallized by heat, so that the surface is projected and recessed, and a sharp projection is generated through an oxide film. Consequently, partially the oxide film is extremely reduced in thickness so that the withstanding pressure between polycrystalline silicon which becomes a substrate and an upper electrode is deteriorated to cause leaking.

This projection of the polycrystalline silicon is hardly caused on the phosphorus highly doped polycrystalline silicon, but easily caused on the boron doped polycrystalline silicon and non-doped polycrystalline silicon.

Fig. 1 shows an example.

As shown in Fig. 1, the reference numeral 1 is a Si substrate, 2 is a SiO_2 film, 3 is an N-type polycrystalline Si, 4 is a P-type polycrystalline Si, 5 is a gate oxide film, 6 is a P^+ polycrystalline Si electrode, 7 is an N^+ polycrystalline Si electrode, 8 is a P^+ polycrystalline Si source, 9 is P^+ polycrystalline Si drain, 10 is an N^+ polycrystalline Si drain, 11 is an N^+ polycrystalline Si source, 12 is an interlayer insulation film, 13 is an Al electrode, and 14 is a projection of the polycrystalline Si.

As shown in Fig. 1, a sharp projection occurs on the surface outside the high density N^+ doped polycrystalline silicon to cause inferior withstanding pressure and leaking.

The invention has effected improvements to overcome the above disadvantages, and it is an object of the invention to improve withstanding pressure and leaking characteristic by forming a nitride film before forming an electrode, and adding a layer where a projection does not grow to a gate film.

Fig. 2 schematically shows a partial section of a three- dimensional semiconductor integrated circuit device formed according to a method of the invention.

The invention will now be described.

As shown in Fig. 2, the reference numeral 21 is a Si substrate, 22 is a SiO_2 film, 23 is an N-type polycrystalline Si, 24 is a P-type polycrystalline Si, 25 is a gate oxide film, 26 is a P^+ polycrystalline Si electrode, 27 is an N^+ polycrystalline Si electrode, 28 is a P^+ polycrystalline Si source, 29 is a P^+ polycrystalline Si drain, 30 is an N^+ polycrystalline Si drain, 31 is an N^+ polycrystalline Si source, 32 is an interlayer insulation film, 33 is an Al electrode, and 34 is a projection of the polycrystalline Si. Further, the reference numeral 35 is a nitride film.

According to the method of the invention described above, a projection of the polycrystalline Si grows only in the gate oxide film, and it does not grow when the nitride film is formed. Withstanding pressure is increased by the nitride film and leaking characteristic is improved.

The optimum thickness of the lower oxide film ranges from 400 to 600Å, and the suitable thickness of the nitride film ranges from about 200 to 400 Å.

Though the description of the invention deals with the case where polycrystalline Si of the SiO_2 film provided on the Si substrate is taken as a substrate, the

same is true for the case of using the polycrystalline Si formed on the insulating substrate itself, and also the same is true for the case of using as the substrate the polycrystalline Si further formed through an insulating film on a film where an element is provided.

Brief Description of the Drawings:

Fig. 1 schematically shows a section of a semiconductor integrated circuit device comprising an MOS field effect transistor using polycrystalline Si as a substrate according to the conventional method; and

Fig. 2 schematically shows a section of a semiconductor integrated circuit device comprising an MOS field effect transistor using polycrystalline Si as a substrate according to the method of the present invention.

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SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE
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APPLICANT(s): SEIKO EPSON CORP [000236] (A Japanese Company or Corporation), JP (Japan)
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ABSTRACT

PURPOSE: To increase dielectric resistance, and to reduce leakage by using a double film consisting of an oxide film and a nitride film as a gate insulating film when the MOSFET is formed only polysilicon shaped onto an insulating layer.
CONSTITUTION: An SiO(sub 2) film 22 is formed onto an Si substrate 21, and an N type polysilicon layer 23 and a P type polysilicon layer 24 are shaped onto the film 22. When the MOSFETs are molded to both silicon layers, the double films 25, the polysilicon sides thereof are composed of the oxide films and the gate sides thereof the nitride films, are used as the gate insulating films. Accordingly, since projections extending from the polysilicon layers do not grow in the sections of the nitride films, the growth of the projections is inhibited, and dielectric resistance is increased. 400-600 angstroms Is optimum as the thickness of the lower oxide films, and approximately 200-400 angstroms is proper as the thickness of the upper nitride films. Such double films are also effective to the polysilicon layers directly shaped onto the insulating substrate.

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Semiconductor integrated circuit - produced by applying two layer structure silicon oxide film and silicon nitride film. NoAbstract
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Number of Countries: 001 Number of Patents: 001
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Title Terms: SEMICONDUCTOR; INTEGRATE; CIRCUIT; PRODUCE; APPLY; TWO; LAYER;STRUCTURE; SILICON; OXIDE; FILM; SILICON; NITRIDE; FILM; NOABSTRACT
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File Segment: CPI; EPI

[redacted]

る。それによって部分的に部分に酸化膜が薄くなり、基体となる多結晶シリコンと上部電極の間の耐圧が低くなり、リークも発生する。

多結晶シリコンのこの現象は、リンを高ドープした多結晶シリコン上には発生しにくいが、ボロンドープした多結晶シリコンとノンドープの多結晶シリコン上には発生しやすい。

第1図に例を示す。

第1図に示すように、1はSi基板であり、2はSiO_2膜、3はN型多結晶Si、4はP型多結晶Si、5はゲート酸化膜、6はP⁺多結晶Si電極、7はN⁺多結晶Si電極、8はP⁺多結晶Siソース、9はP⁺多結晶Siドレイン、10はN⁺多結晶Siドレイン、11はN⁺多結晶Siソース、12は層間絶縁膜、13はAl電極、14は多結晶Siの突起である。

第1図に示されているように、N⁺に高くドープされた多結晶シリコン以外の所の表面にはするどい突起が出現し、耐圧及びリーク不良となっている。

本発明は以上のような欠点について改良を加えたもので、本発明の目的は電極形成する前に、酸化膜を形成し、突起の成長しない膜をゲート膜に加えて耐圧及びリーク特性を改善することを目的としている。

第2図に、本発明の方法によって形成された三次元半導体集積回路装置の部分的断面略図を示し以下に本発明について説明する。

第2図に示すように、21はSi基板であり、22はSiO_2膜、23はN型多結晶Si、24はP型多結晶Si、25はゲイト酸化膜、26はP⁺多結晶Si電極、27はN⁺多結晶Si電極、28はP⁺多結晶Siソース、29はP⁺多結晶Siドレイン、30はN⁺多結晶Siドレイン、31はN⁺多結晶Siソース、32は層間絶縁膜、33はAl電極、34は多結晶Siの突起である。さらに35は酸化膜である。

以上の本発明の方法によると、多結晶Siの突起はゲート酸化膜中のみで成長し、酸化膜を形成する時には成長しなくなる。そして酸化膜によって耐圧がよし、リーク特性が改善される。

下の酸化膜は400～600Åが最適であり、酸化膜の厚さは200～400Å程度が適している。

本発明はSi基板上にもうけたSiO_2膜の多結晶Siを基体とした場合について説明したが、絶縁基板そのものの上に形成した多結晶Siを用いた場合も同様であり、素子がもうけられたさらにその上に絶縁膜をかいして形成された多結晶Siを基体として用いた場合も同様である。

4. 図面の簡単な説明

第1図は従来方法による多結晶Siを基体としたMOS電界効果トランジスタを構成要素とする半導体集積回路装置の断面略図である。

第2図は本発明の方法による多結晶Siを基体としたMOS電界効果トランジスタを構成要素とする半導体集積回路装置の断面略図である。

以　上

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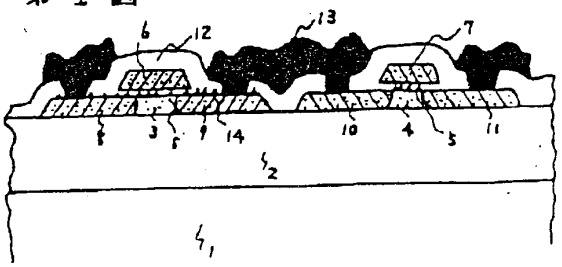
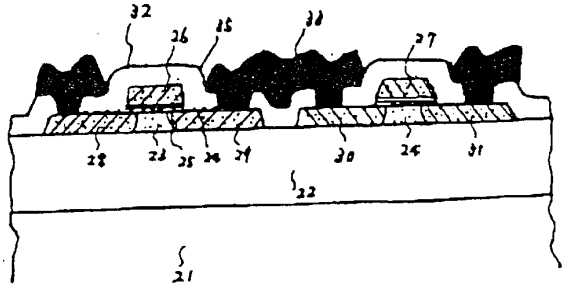
第1図



第2図



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//H 01 L 29/62			発明の数 1
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⑭半導体集積回路装置

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明　　細　　書

1. 発明の名称

半導体集積回路装置

2. 特許請求の範囲

1) 絶縁膜上に形成した多結晶シリコンを基体としてMOS型電界効果トランジスタを形成してなる半導体集積回路装置において、ゲート部の絶縁膜としてシリコン酸化膜とシリコン窒化膜の二層構造とした事を特徴とする半導体集積回路装置。

2) 前記シリコン酸化膜の膜厚を50Åから1000Åとした事を特徴とする特許請求の範囲第1項記載の半導体集積回路装置。

3) 前記シリコン窒化膜の膜厚を30Åから1000Åとした事を特徴とする特許請求の範囲第1項及び第2項記載の半導体集積回路装置。

3. 発明の詳細な説明

本発明は、絶縁膜上にもうけた多結晶シリコンを基体として用いたMOS型電界効果トランジスタに関し、そのゲート絶縁膜に関する。

半導体集積回路装置は年々微細化が進められ、その中でもMOS型電界効果トランジスタを構成要素とする半導体集積回路装置の微細化にはめざましいものがある。アライナー技術、エッチング技術、デバイス技術等はさらに進みつつあり、微細化も2μルールを割り、量産レベルでの限界に近かずきつつある。前々から素子を上につみあげる三次元半導体集積回路装置の構想があり、各方面で様々検討されてきたが、ここにいたって、にわかに活気を呈し始めているのが現状である。

現在、開発を試みられているのはMOS型電界効果トランジスタを構成要素とするものである。現在、実用化にさいしては種々の問題があるが、その中で特に大きな問題は、多結晶シリコン上のゲート部の耐圧が低い事である。この原因は多結晶シリコンの表面を酸化すると多結晶シリコンが熱によって結晶化が進み、表面に凸凹が生じると同じに、するどい突部が酸化膜中を通して発生す